MEMORY DEVICE AND METHOD OF SIMULTANEOUS FABRICATION OF CORE AND PERIPHERY OF SAME

ABSTRACT OF THE DISCLOSURE

A method of fabricating a memory device having a core region of double-bit memory cells and a periphery region of logic circuitry includes forming a dielectric stack over the core and periphery areas of a semiconductor substrate and removing the dielectric stack from the periphery region. A gate dielectric is formed over the periphery area, followed by a first conductive layer over the core and periphery areas. After the formation and thermal processing of the gate dielectric, bitlines, which serve as source and drain regions, are implanted into the core area. Formation of the bitlines after the gate dielectric layer reduces lateral bitline diffusion and reduces short channel effects.

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